REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of February 20, 2003, and is believed to be fully responsive thereto for reasons set forth below in greater detail.

Responsive to the objection to the drawings, corrected substitute drawings for Figures 8-10 are submitted herewith, adding the legend PRIOR ART to Figures 8-10.

Claims 6-10 and 13 have been amended to correct an apparent error in claim 6, and to clarify the subject matter of claims 7-10 and 13.

Reconsideration is respectfully requested of the rejection of:

claims 1-2, and 7-14 under 35 U.S.C. 102(b) as being anticipated by Suzuki et al ('030);

claims 3-6 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Tomita ('061); and

claims 15-16 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Takahashi et al ('300).

Initially, the present invention operates by applying pulse signals from a plurality of storage capacitor lines to a plurality of storage capacitors, and optionally by applying pulse signals from a plurality of signal lines to the plurality of storage capacitors, via a plurality of switching elements.

Independent claims 1 and 2 both specify "applying pulse signals from said plurality of storage capacitor lines to said plurality of storage capacitors", and independent

claim1 additionally specifies "applying pulse signals from said plurality of signal lines to said plurality of storage capacitors via said plurality of switching elements."

Similarly, independent claims 13 and 14 both specify a pulse signal generating device connected to said storage capacitor lines in order to apply the pulse signals respectively to said plurality of storage capacitor; and independent claim 14 additionally specifies a pulse signal generating device connected to said signal lines in order to apply the pulse signal to said plurality of storage capacitors.

In all of the prior art rejections herein, the Examiner has misconstrued the primary reference Suzuki et al ('030) as Suzuki et al does not apply pulse signals through the storage capacitor lines to the storage capacitors.

The prior art rejection and explanation of Suzuki et al ('030) on pages 2-4 of the Official Action refers to Figure 7 of Suzuki et al ('030) and storage capacitors 8 and storage capacitor lines 33, and the applicants agree therewith.

However, the explanations of the operation of the circuit of Figure 7 makes it perfectly clear that the storage capacitor lines 33 are only used to read signals from the storage capacitors, and are not used to apply pulse signals to the storage capacitors.

Refer to the operation as explained at column 9, line 67, to column 10, line 37,

"As shown in FIG. 7, the inspection scan switching circuit 34A is connected to the video signal input terminal line 32. One of the switch terminals 34a of the inspection scan switching circuit 34A is connected to the inspection signal writing power source 36. The voltage applied from the writing power source 36 is about the same as the voltage at the time of actually driving the LCD. The other scan switching circuit 34b of the inspection scan switching circuit 34A is connected to the reference voltage (ground).

The scan switching circuit 34A operates in synchronization with the inspection scan switching circuit 34B connected to a common electrode terminal line 33. The common electrode terminal line 33 has connected to it a decision means 40 through an I/V amplifier 38. The decision means 40 is constituted by, for example, an image processing apparatus and analyzes the pixel information input through the I/V amplifier 38.

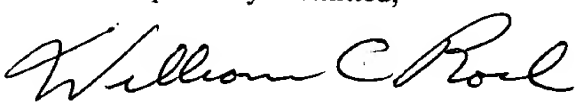
The inspection scan switching circuit 34A is constituted so as to switch between connection to the terminal 34a and connection to the terminal 34b at a predetermined cycle. Further, in synchronization with the operation of the inspection scan switching circuit 34A, the inspection scan switching circuit 34B switches between the case of connection to the reference voltage and the case of opening the connection to the reference voltage. That is, a charge is successively stored in the capacitor elements 8 from the inspection signal writing power source 36 through the video input terminal line 32 and data lines 28. When wiring the inspection signal, the scan switching circuit 34B is connected to the reference voltage and the potential is not read out by the decision means 40. Further, when the scan switching circuit 34A is switched to connect to the switching terminal 34b, the scan switching circuit 34B becomes open and the charge stored in the capacitor elements 8 is successively read out (through the common electrode terminal line 33 – the storage capacitor line); the discharge current is converted to voltage, and the result is monitored by the decision means 40.

Moreover, the pulse signals of Figure 3a referred to in the Office Action are video field (timing) signals, and are not applied to the storage capacitors.

Accordingly, each of independent claims 1, 2, 13 and 14 is believed to readily distinguish over the prior art.

This application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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